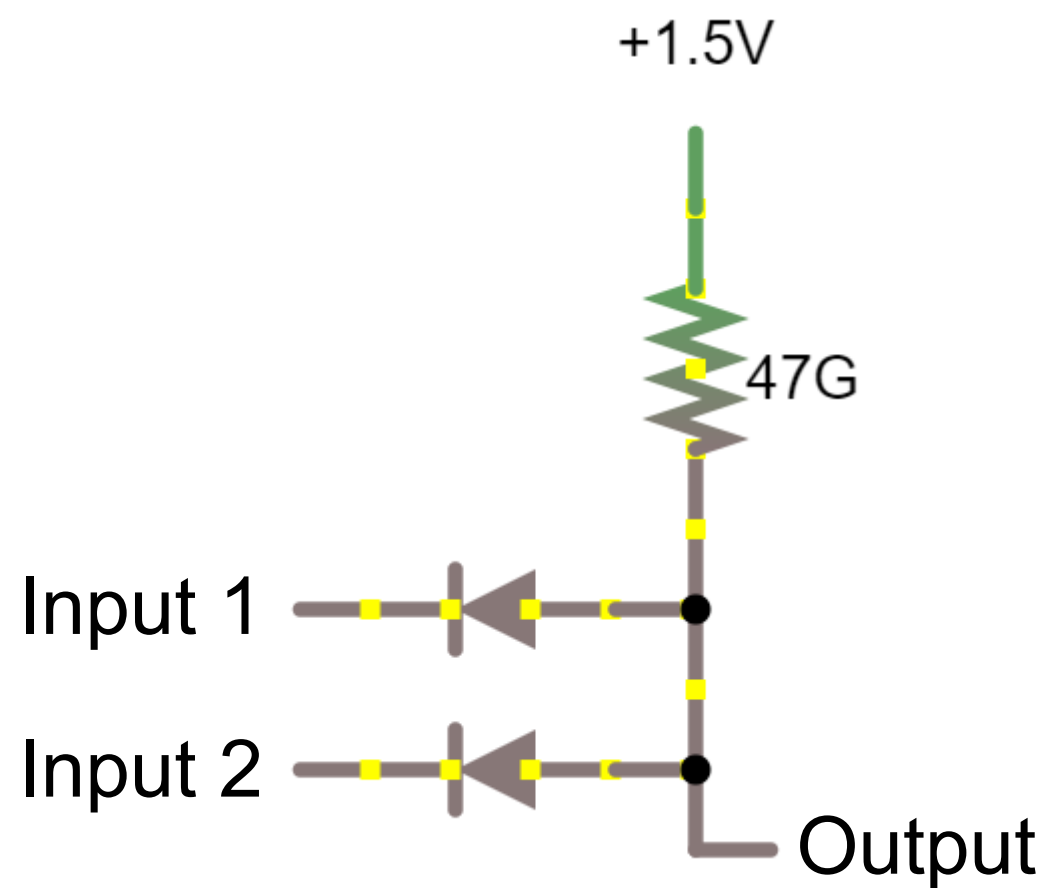


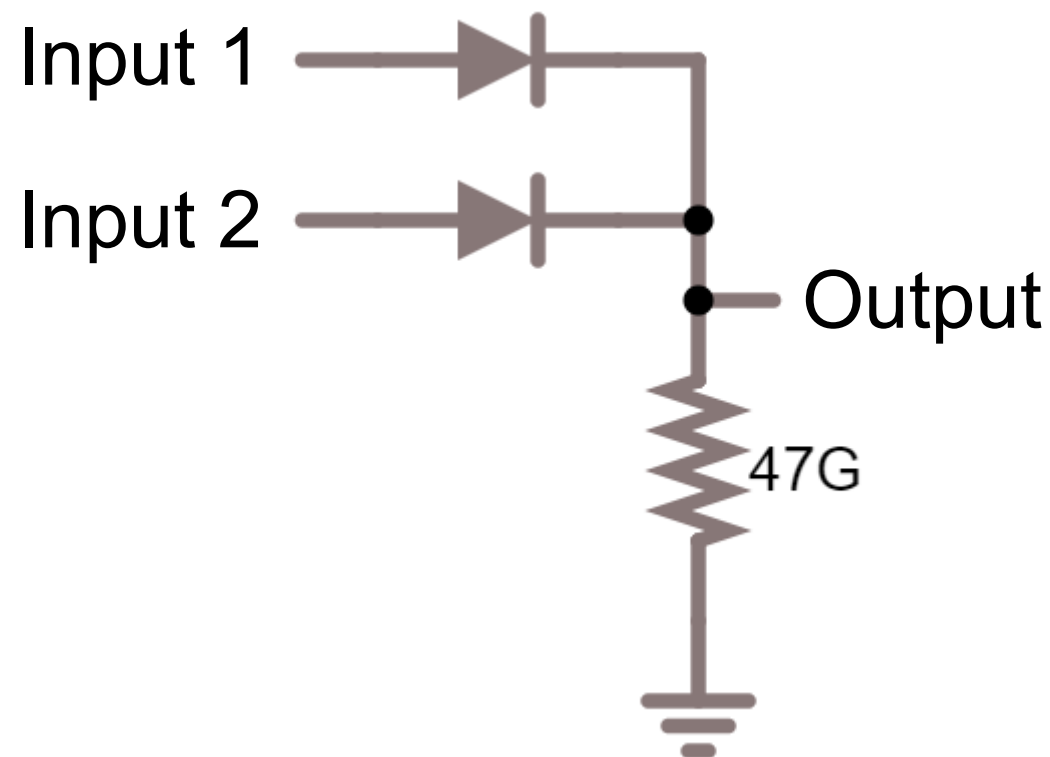
a

AND Logic



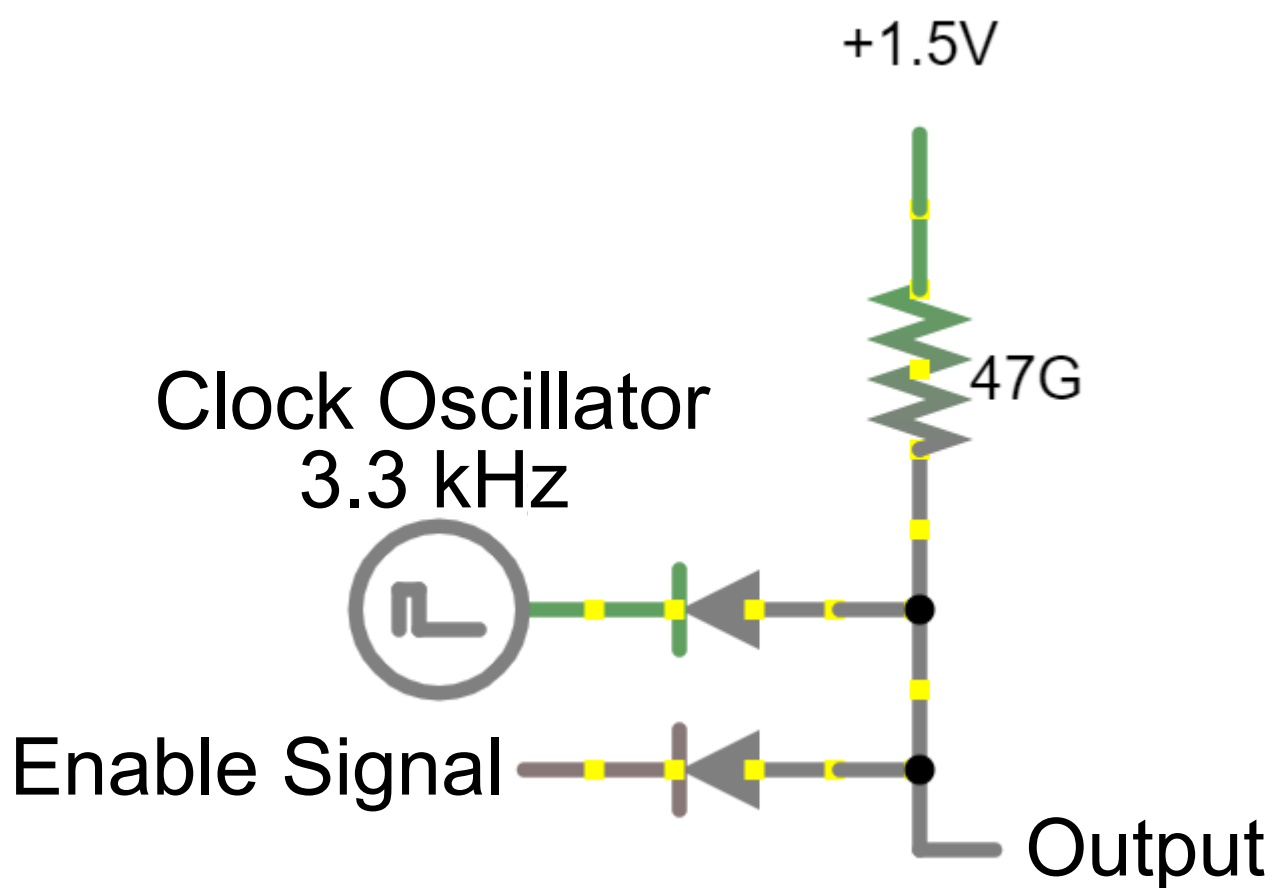
b

OR Logic



c

AND Logic Pulse Modulation



d

OR Logic Pulse Modulation

